In the Claims:

Claims 1-4 (Cancelled).

5. (Previously Presented) A computer system comprising:

a master apparatus; and

a slave apparatus for communicating asynchronously with said master apparatus and communicating via a universal serial bus (USB) protocol, said slave apparatus comprising

a sending/receiving circuit for sending and receiving binary information to and from said master apparatus and supplying status signals based thereon,

a plurality of state latches and control circuitry cooperating therewith for receiving the status signals from said sending/receiving circuit and supplying state signals of said sending/receiving circuit based thereon,

a microprocessor for processing applications of said slave apparatus and also for processing the binary information received by said sending/receiving circuit when an interruption signal is supplied, and

an interruption state latch and a control circuit cooperating therewith for supplying the interruption signal to said microprocessor once the start of a new message from said master apparatus has been acknowledged and recorded by said sending/receiving circuit,

said sending/receiving circuit also acknowledging the start of a following message from said master apparatus while the interruption signal is supplied.

6. (Previously presented) The computer system of Claim 5 wherein said control circuit for controlling said interruption state latch comprises at least one logic circuit for receiving the status signals from said sending/receiving circuit and setting said interruption state latch to a predetermined logic level to indicate a microprocessor interruption request.

7. (Previously presented) The computer system of Claim 5 wherein said control circuitry for controlling said state latches prevents the binary information from said sending/receiving circuit from being written into said plurality of state latches during receipt of the start of the new message and during the presence of the interruption signal.

8. (Previously presented) The computer system of Claim 5 wherein said master apparatus comprises a central processing unit.

9. (Previously presented) The computer system of Claim 5 wherein said slave apparatus comprises a computer peripheral device.

10. (Previously presented) The computer system of Claim 5 further comprising a cable connecting said master apparatus and said slave apparatus.

11. (Previously Presented) A computer system comprising:

a master apparatus; and

a slave apparatus for communicating asynchronously with said master apparatus and comprising

a sending/receiving circuit for sending and receiving binary information to and from said master apparatus and supplying status signals based thereon,

a plurality of state latches and control circuitry cooperating therewith for receiving the status signals from said sending/receiving circuit and supplying state signals of said sending/receiving circuit based thereon,

a microprocessor for processing applications of said slave apparatus and also for processing the binary information received by said sending/receiving circuit when an interruption signal is supplied, and

an interruption state latch for supplying the interruption signal to said microprocessor once the start of a new message from said master apparatus has been acknowledged and recorded by said sending/receiving circuit,

said sending/receiving circuit also acknowledging the start of a following message from said master apparatus while the interruption signal is supplied,

said control circuitry for controlling said state latches preventing the binary information from said sending/receiving circuit from being written into said plurality of state latches during receipt of the start of the new message and during the presence of the interruption signal.

12. (Previously presented) The computer system of Claim 11 wherein said master apparatus and said slave apparatus communicate via a universal serial bus (USB) protocol.

13. (Previously presented) The computer system of Claim 11 further comprising at least one logic circuit for receiving the status signals from said sending/receiving circuit and setting said interruption state latch to a predetermined logic level to indicate a microprocessor interruption request.

14. (Previously presented) The computer system of Claim 11 wherein said master apparatus comprises a central processing unit.

15. (Previously presented) The computer system of Claim 11 wherein said slave apparatus comprises a computer peripheral.

16. (Previously presented) The computer system of Claim 11 further comprising a cable connecting said master apparatus and said slave apparatus.

17. (Previously Presented) A slave apparatus for communicating asynchronously with a master apparatus via a universal serial bus (USB) protocol, said slave apparatus comprising:

a sending/receiving circuit for sending and receiving binary information to and from the master apparatus and supplying status signals based thereon;

a plurality of state latches and control circuitry cooperating therewith for receiving the status signals from said sending/receiving circuit and supplying state signals of said sending/receiving circuit based thereon;

a microprocessor for processing applications of the slave apparatus and also for processing the binary information received by said sending/receiving circuit when an interruption signal is supplied; and

an interruption state latch and a control circuit cooperating therewith for supplying the interruption signal to said microprocessor once the start of a new message from the master apparatus has been acknowledged and recorded by said sending/receiving circuit;

said sending/receiving circuit also acknowledging the start of a following message from the master apparatus while the interrupt signal is supplied.

18. (Previously presented) The slave apparatus of Claim 17 wherein said control circuit for controlling said interruption state latch comprises at least one logic circuit for receiving the status signals from said sending/receiving circuit and setting said interruption state latch to a

predetermined logic level to indicate a microprocessor interruption request.

19. (Previously presented) The slave apparatus of Claim 17 wherein said control circuitry for controlling said state latches prevents the binary information from said microprocessor from being written into said plurality of state latches during receipt of the start of the new message and during the presence of the interruption signal.

20. (Previously Presented) A method of processing interruptions in a slave apparatus for communicating asynchronously with a master apparatus via a universal serial bus (USB) protocol, the method comprising:

sending and receiving binary information to and from the master apparatus via a sending/receiving circuit and supplying status signals based thereon;

generating state signals of the sending/receiving circuit based upon the status signals;

processing applications of the slave apparatus and also processing the binary information received by the sending/receiving circuit when an interruption signal is supplied;

supplying the interruption signal to a microprocessor of the slave apparatus once the start of a new message from the master apparatus has been acknowledged and recorded by the sending/receiving circuit; and

sending an acknowledgement from the sending/receiving circuit to the master apparatus

acknowledging the start of a following message from the master apparatus while the interrupt signal is supplied.

21. (Previously presented) The method of Claim 20 wherein supplying the interruption signal comprises setting an interruption state latch to a predetermined logic level based upon the status signals to indicate a microprocessor interruption request.

22. (Cancelled).